

FIS920010074  
I26-0016-D

## REMARKS

Claims 1-7 and 9 were pending in the present application.

Claim 1 has been amended, and Claim 9 has been canceled, leaving Claims 1-4, and 6-7 for further consideration in the present amendment. Support for the amendments to Claim 1 can be found at least in the examples.

Reconsideration and allowance of the claims is respectfully requested in view of the following remarks.

### Claim Rejections Under 35 U.S.C. § 102

A. Claims 1-7 and 9 stand rejected under 35 U.S.C. §102(b), as allegedly anticipated by U.S. Patent No. 4,541,168 to Galie et al. (hereafter “*Galie*”). Applicants respectfully traverse.

To anticipate a claim under 35 U.S.C. §102, a single source must contain all of the elements of the claim. *Lewmar Marine Inc. v. Barent, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766, 1768 (Fed. Cir. 1987), *cert. denied*, 484 U.S. 1007 (1988).

*Galie* does not disclose Applicants’ claimed process of cleaning a semiconductor material surface of a partially manufactured integrated circuit subsequent to implantation of dopant ions into the surface and prior to any other semiconductor manufacturing process. Rather, *Galie* discloses a multi-step process for forming metal contact studs. Subsequent to ion implantation, *Galie* passivates an ion implanted structure with a passivation layer as noted below.

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The structure is comprised of a p- boron doped substrate 11 having a blanket N<sup>+</sup> subcollector 12 and an N<sup>-</sup> epitaxial layer 13 thereon. The latter includes a conventional NPN transistor structure comprised of: an N<sup>+</sup> reach through 14, a P base region 15 and an N<sup>+</sup> emitter region. The structure is passivated with a composite SiO<sub>2</sub> ( $\approx$ 300nm) and Si<sub>3</sub>N<sub>4</sub> ( $\approx$ 100nm) respectively referenced 17 and 18.

(Galie, Col. 3, ll. 51-57)

There is no disclosure of a process of cleaning a semiconductor material surface of a partially manufactured integrated circuit subsequent to implantation of dopant ions into the surface and prior to any other semiconductor manufacturing process as claimed by Applicants. In Galie, any mention to acetone is in reference to a contact lift-off step, which occurs subsequent to numerous intervening steps in the process following ion implantation. Moreover, Applicants positively recite that “wherein coating the semiconductor material surface occurs prior to formation of a barrier layer on the surface” as in Claim 1.

In view of the foregoing, the rejection is respectfully requested to be withdrawn.

B. Claims 1-7 and 9 stand rejected under 35 U.S.C. §102(b), as allegedly being anticipated by U.S. Patent No. 3,599,323 to Saxena et al. (hereafter “*Saxena*”). Applicants respectfully traverse.

*Saxena* is directed to fabrication of a Schottky barrier diode. The process includes growing an epitaxial P-type on a heavily doped P<sup>++</sup> silicon wafer. Like Galie above, the wafer is then oxidized to form a passivation layer and then using standard lithographic techniques, chromium is selectively deposited by vapor deposition. Prior to forming the chromium-silicon interface, the substrate is first cleaned with trichloroethylene, acetone and deionized water.

There is no disclosure of a cleaning process comprising coating the semiconductor material surface containing the dopant ions with a solution consisting of a non-aqueous organic solvent selected from the group consisting of ketones, polyhydric alcohols, cyclic ethers and esters, wherein coating the semiconductor material surface is subsequent to

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implantation of dopant ions into the surface, occurs prior to formation of a barrier layer on the surface, and prior to any other semiconductor manufacturing process. Subsequent to ion implantation, Saxena discloses forming a passivation layer.

In view of the foregoing, the rejection is requested to be withdrawn.

It is believed that the foregoing amendments and remarks fully comply with the Office Action and that the claims herein should now be allowable to Applicants. Accordingly, reconsideration and allowance is requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 09-0458 maintained by Assignee.

Respectfully submitted,

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